WHAT IS CLAIMED IS:

1. A CMOS basic cell comprising:

an N-channel transistor region and a P-channel transistor region isolated from each other by an insulating film on a semiconductor substrate; and

an interconnect pattern extending along a direction perpendicular to a boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region,

wherein said interconnect pattern is formed in an uppermost interconnect layer among one, two or more interconnect layers of said CMOS basic cell.

2. A CMOS basic cell comprising:

an N-channel transistor region and a P-channel transistor region isolated from each other by an insulating film on a semiconductor substrate; and

an interconnect pattern extending along a direction parallel to a boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region,

wherein said interconnect pattern is formed in an uppermost interconnect layer among one, two or more interconnect layers of said CMOS basic cell.

3. A CMOS basic cell comprising:

an N-channel transistor region and a P-channel transistor region isolated from each other by an insulating film on a semiconductor substrate; and

an interconnect pattern extending along a direction parallel to a boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region to be used for connection to an interconnect pattern of another adjacent basic cell,

wherein said interconnect pattern is formed in an uppermost interconnect layer among one, two or more interconnect layers of said CMOS basic cell.

4. A CMOS basic cell comprising:

an N-channel transistor region and a P-channel transistor region isolated from each other by an insulating film on a semiconductor substrate;

an interconnect pattern extending along a direction perpendicular to a boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region; and

another interconnect pattern extending along a direction parallel to the boundary between said N-channel transistor region and said P-channel transistor region and

provided independently of said N-channel transistor region and said P-channel transistor region,

wherein said interconnect patterns are formed in an uppermost interconnect layer among one, two or more interconnect layers of said CMOS basic cell.

5. A CMOS basic cell comprising:

an N-channel transistor region and a P-channel transistor region isolated from each other by an insulating film on a semiconductor substrate;

an interconnect pattern extending along a direction parallel to a boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region; and

another interconnect pattern extending along the direction parallel to the boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region to be used for connection to an interconnect pattern of another adjacent basic cell,

wherein said interconnect patterns are formed in an uppermost interconnect layer among one, two or more interconnect layers of said CMOS basic cell.

6. A CMOS basic cell comprising:

an N-channel transistor region and a P-channel transistor region isolated from each other by an insulating film on a semiconductor substrate;

an interconnect pattern extending along a direction perpendicular to a boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region; and

another interconnect pattern extending along a direction parallel to the boundary between said N-channel transistor region and said P-channel transistor region and provided independently of said N-channel transistor region and said P-channel transistor region to be used for connection to an interconnect pattern of another adjacent basic cell,

wherein said interconnect patterns are formed in an uppermost interconnect layer among one, two or more interconnect layers of said CMOS basic cell.

7. The CMOS basic cell of any of Claims 1 through 6, further comprising a fixed interconnect region where a power supply interconnect and a ground interconnect are provided,

wherein said interconnect pattern is provided in said fixed interconnect region.

8. A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and

additional interconnect layers respectively provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells of Claim 1, 2, 3, 4, 5 or 6 on a semiconductor substrate; and

realizing a logic circuit including a clock signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said additional interconnect layers.

9. A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and additional interconnect layers respectively provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells of Claim 1, 2, 3, 4, 5 or 6 on a semiconductor substrate; and

realizing a logic circuit including transistors connected to each other in parallel by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said additional interconnect layers.

10. A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and additional interconnect layers respectively provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells of Claim 1, 2, 3, 4, 5 or 6 on a semiconductor substrate; and

realizing a composite logic circuit by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said additional interconnect layers.

11. A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and additional interconnect layers respectively provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells of Claim 1, 2, 3, 4, 5 or 6 on a semiconductor substrate; and

realizing a logic circuit including a control signal line by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said additional interconnect layers.

12. A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells and additional interconnect layers respectively provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells of Claim 1, 2, 3, 4, 5 or 6 on a semiconductor substrate; and

realizing a logic circuit for a memory by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said additional interconnect layers.

13. A method for fabricating a gate array semiconductor

integrated circuit including a plurality of basic cells and additional interconnect layers respectively provided above said basic cells, comprising the steps of:

arranging a plurality of CMOS basic cells of Claim 1, 2, 3, 4, 5 or 6 on a semiconductor substrate; and

realizing a flip-flop circuit having a scan test function by using said interconnect patterns formed in the uppermost interconnect layers of said CMOS basic cells and said additional interconnect layers.

14. A CMOS basic cell to be used with other basic cells having the same structure disposed on right and left hand sides thereof, comprising:

an N-channel transistor and a P-channel transistor formed on a semiconductor substrate,

wherein a gate of at least one of said N-channel transistor and said P-channel transistor is in a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof.

15. A CMOS basic cell to be used with other basic cells having the same structure disposed on right and left hand sides thereof, comprising:

an N-channel transistor and a P-channel transistor formed on a semiconductor substrate,

wherein a diffusion region of at least one of said N-

channel transistor and said P-channel transistor is in a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof.

16. A CMOS basic cell to be used with other basic cells having the same structure disposed on right and left hand sides thereof, comprising:

an N-channel transistor and a P-channel transistor formed on a semiconductor substrate,

wherein a gate of at least one of said N-channel transistor and said P-channel transistor is in a hooked shape including a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof, and

a diffusion region of at least one of said N-channel transistor and said P-channel transistor is in a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof.

17. The CMOS basic cell of Claim 16,

wherein a first N-channel transistor and a first P-channel transistor are formed to extend along a vertical direction,

a second N-channel transistor is disposed on a side of

said first N-channel transistor and a second P-channel transistor is disposed on a side of said first P-channel transistor, and

a gate of each of said first and second N-channel transistors and said first and second P-channel transistors is formed in the hooked shape.

18. The CMOS basic cell of Claim 17,

wherein the gates of said first and second N-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when seen along the vertical direction from one position in a horizontal direction, and

the gates of said first and second P-channel transistors are disposed in a manner that said first bent part of one gate overlaps said second bent part of the other gate when seen along the vertical direction from one position in the horizontal direction.

19. The CMOS basic cell of Claim 17,

wherein said first and second N-channel transistors share one diffusion region and said first and second P-channel transistors share one diffusion region,

each of said diffusion regions is divided into a shared diffusion region shared by said first and second N-channel or P-channel transistors and positioned between the gates of said first and second N-channel or P-channel transistors; a

first dedicated diffusion region positioned on a side of said gate of said first N-channel or P-channel transistor opposite to said shared diffusion region; and a second dedicated diffusion region positioned on a side of said gate of said second N-channel or P-channel transistor opposite to said shared diffusion region,

said first bent part is formed in said first dedicated diffusion region, and

said second bent part is formed in said second dedicated diffusion region.

20. The CMOS basic cell of Claim 14, 15, 16, 17, 18 or 19, comprising, outside of a transistor region where said N-channel transistor and said P-channel transistor are disposed, a fixed interconnect region where a power supply interconnect and a ground interconnect are disposed.

21. A method for fabricating a gate array semiconductor integrated circuit including a plurality of basic cells arranged in a horizontal direction, comprising a step of arranging a plurality of CMOS basic cells of Claim 14, 15, 16, 17, 18 or 19 in the horizontal direction in a manner that said first bent part of one CMOS basic cell overlaps said second bent part of another adjacent CMOS basic cell when seen along a vertical direction from one position in a horizontal direction.

add a1
add c3